Amendments to the Specification:

Please replace the paragraph at page 3, lines 11-17 with the following amended paragraph:

In one embodiment, the distributed data processing resources are disposed on logic boards having emulation ICs that include the reconfigurable logic and interconnect resources. In other embodiments, at least some of the distributed data processing resources are disposed on the emulation ICs. The board and IC disposed ~~distribtued~~ distributed data processing resources cooperatively perform the earlier mentioned distributed and corresponding generation of ~~configruation~~ configuration signals and interconnect routing determination.

Please replace the paragraph at page 7, lines 3-8, with the following amended paragraph:

Emulation ICs **104**, in particular, their on-chip reconfigurable logic and interconnect resources, as in prior art "FPGAs", are used to "realize" the netlists of an IC design to be emulated. In various embodiment, each emulation IC **104** may advantageously include integrated debugging facilities, such as those included with enhanced "FPGAs" described in USP 5,777,489, and co-pending U.S. Patent Application number ~~<insert the CIP number here>~~09/404,925, now U.S. Patent No. 6,265,894, to be described more fully below.

Please replace the paragraph extending from page 9, line 13 to page 10, line 2, with the following amended paragraph:

Referring now to **Figures 2a-2b**, wherein two block diagrams illustrating an emulation IC **104** in further details, in accordance with one embodiment, are shown. As illustrated in **Fig. 2a**, emulation IC **104** includes reconfigurable LEs (RLR) **202**, reconfigurable interconnects (RIN)

204, emulation memory (MEM) **206**, debugging resources (DBR) **208**, context or state elements (CTX) **210**, and configuration registers (CR) **212** and **214** coupled to each other as shown. Reconfigurable LEs **202**, emulation memory **206** and context/state elements **210** are used to "realize" circuit elements of the netlists of an assigned partition of an IC design to be emulated. In particular, reconfigurable LEs **202** are used to "realize" the combinatorial logic of the netlists of the assigned partition of an IC design to be emulated. Context/state elements **210** are used to "realize" state elements of the ~~netliest~~ netlist of the assigned partition of the IC design to be emulated, such as flip-flops, and so forth, whereas emulation memory **206** are used to "realize" storage elements of the netlists of the assigned partition of the IC design to be emulated. Reconfigurable interconnects **204** are used to ~~reconfigurbaly~~ reconfigurably couple LEs **202**, memory **206** and so forth.

Please replace the paragraph at p. 10, lines 3-9 with the following amended paragraph:

In various embodiments, configuration of these elements, including determination of the interconnect routing, to emulate the netlists of an assigned partition of an IC design, reading of state data of state elements, including determination of which state elements to read, capturing of signal states, ~~includingre-creation~~including re-creation of "unobservable" signals, are locally (i.e. distributively) performed by data processing resources **102** of the host logic board **100**, to be described more fully below.

Please replace the paragraph at page 10, lines 20-23, with the following amended paragraph:

Except for the novel manner that on-board data processing resources **102** control and operate these enumerated elements of emulation IC **104**, the various enumerated elements of emulation IC **104** are otherwise known in the art, and accordingly will not be further described.